REMARKS

Attached hereto is an Excess Claims Fee letter for two excess independent claims.

It is noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Claims 2-25 are all of the claims pending in the present Application. Claim 1 is canceled above. Claims 7-21 are allowed. Claims 1-6 and 23 stand rejected under 35 USC §102(e) as unpatentable anticipated by US Patent 6,499,048 to Williams. Claims 24 and 25 stand rejected under 35 USC §103(a) as unpatentable over Williams.

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

As described, for example, by independent claim 4 and similarly in claims 23-25, the present invention is directed to a method of multithread processing on a computer. A first thread is processed on a first component. The first component is capable of simultaneously executing at least two threads. The first thread is also processed on a second component, and the second component is also capable of simultaneously executing at least two threads.

A result of the processing on the first component is compared with a result of the processing on the second component. The processing of the thread on the second component is performed at a priority lower than a priority of the processing of the thread on the first component.

Since lower priority generally results in slower execution, this scheme of prioritization of the present invention has the advantage of intentionally keeping one thread on one component behind its sister thread on the other component. By intentionally making one thread lag behind, the efficiency of the combined computing resources of the two components can be enhanced, since the lagging thread processing can take advantage of the processing experience of the same thread as executed by the other component.

II. THE PRIOR ART REJECTIONS

The Examiner alleges that Williams anticipates claims 1-6 and 23 and renders obvious claims 24 and 25. Applicants respectfully disagree.

To begin with, relative to now-canceled claim 1, although the description of the alternate configuration at lines 7-9 of column 2 ("The invention also finds application to a plurality of processing units, each configured to process at least one thread.") might arguably be considered as related to the description of original independent claims 1 and 23-25, Applicants submit that the evaluation in the rejection for claims 3, 4, and 6 is clearly incorrect, as would be readily apparent to one of ordinary skill in the art.

In general, Applicants submit that the reason that Williams fails to teach or suggest these features of the present invention is that this reference teaches that fault detection between two processors requires that the two processors be synchronized in order to compare results at any one point in time (see, e.g., lines 20-38 of column 5).

In contrast, the present invention intentionally introduces a lag on one of the two processors, using a number of techniques. The benefit of this fundamentally different strategy is that the inventors have realized that such lag allows the overall efficiency to be increased, since both processors will be allowed to operate at basically full performance. That is, in the teaching of the present invention, the stalling of the faster processor, as done in Williams to keep the two processors synchronized, is not desireable, since such stalling would decrease overall efficiency.

Applicants submit that these fundamentally different techniques are clearly distingishable in at least independent claims 3, 4, 6, and 23-25.

That is, relative to the current rejections for claims 3 and 23, the Examiner points to line 64 of column 3 through line 4 of column 4. However, Applicants submit that, to one of ordinary skill in the art, this description fails to heed the plain meaning of the claim language.

The description in the claimed invention for the enabling/disabling signal refers to the enabling/disabling of the comparison scheme. Thus, in the present invention, the two components (processing sets) can continue to function after disablement, except that their results are no longer compared. For example, the two processors may be signaled to start

working on two different threads or problems. Williams does not teach or suggest this feature.

That is, the disablement in Williams refers to the elimination of one processor because of a fault detected, an entirely different concept. In Williams, that failed processor presumably stops producing any, or at least any useful, results.

Hence, turning to the clear language of the claims, in Williams there is no teaching or suggestion of: "... providing an input to enable or to disable said comparing", as required by claim 3.

Relative to the rejection for claim 4, applicants again respectfully submit that this technique is not taught or suggested in Williams. The Examiner points to the description in Williams at lines 34-37 of column 5. However, Applicants submit that, to one of ordinary skill in the art, this description clearly refers to the stalling technique used in Williams, a concept quite different from the prioritization used in the present invention.

That is, the description in the claimed invention refers to the priority of processing a thread on a component that executes multiple distinct threads. This description in Williams refers to the relative speed (and stalling, as appropriate) of versions of the same thread executing on multiple components.

Lower priority generally would result in slower execution. The aim of the scheme in the present invention is to use the priority mechanism to keep one thread on one component always behind its sister thread on the other component. It is noted that this concept is fundamentally contrary to the aim in Williams to keep the two threads synchronized. Moreover, Williams does not distinguish threads because it allows either thread to get ahead of the other before the faster thread is stalled.

Hence, turning to the clear language of the claims, in Williams there is no teaching or suggestion of: "... wherein said processing said thread on said second component is performed at a priority lower than a priority of said processing said thread on said first component... ", as required by independent claim 4. Independent claims 23-25 have similar language.

Finally, relative to the rejection for claim 6, Applicants respectfully submit that the information sharing between threads is not at all taught or suggested in Williams. At most,

Williams merely compares the result of the two threads, an entirely different concept from sharing of information that the higher priority thread has learned during its processing of the thread so that the lower priority processing can take advantage of this information.

As an example, the information about the actual direction of branches generated by one component may be used as branch prediction by the other component.

In contrast, line 35 of column 6 of Williams is not referring to this type of shared information or data. Rather, it is referring to a control signal from the monitor (not even from the other processing set) that controls the activity of a processing set. This is an entirely different concept.

Hence, turning to the clear language of the claim, in Williams there is no teaching or suggestion for"... wherein said processing said thread on said second component uses information available from said processing said thread on said first component", as required by claim 6.

For the reasons stated above, Applicants respectfully submit that the claimed invention is fully patentable over the cited reference Williams.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicants submit that claims 2-25, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

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